REMARKS

The above amendments and following remarks are submitted in response to the First Official Action of the Examiner mailed May 8, 2003. Having addressed all objections and grounds of rejection, claims 1-20, being all the pending claims, are now deemed in condition for allowance. Entry of these amendments and reconsideration to that end is respectfully requested.

The Examiner has objected to the drawings. Specifically, the Examiner has found that Figs. 1-3 contain only prior art under MPEP 608.02(g). This was not Applicant's intention nor does Applicant believe that the specification supports the Examiner's conclusion. However, the Examiner states:

> The Examiner notes that on pages 6-10 of Applicant's specification that figures 1-3 are described as typical and legacy.

Though the figures are described as containing "legacy" elements, this is not deemed to render the corresponding figure prior art.

Figs. 1-3 show the application of the DCP in providing the interface amongst various legacy system elements. To the extent that the illustrated DCP is implemented utilizing Applicant's novel emulation approach, which is Applicant's preferred embodiment, the system is not "prior art" in the sense of MPEP

608.02(g). Nevertheless, if the language of Applicant's specification has caused the confusion, it is deemed appropriate that the specification be amended as provided above to alleviate this alleged ambiguity. No new matter has been added. Furthermore, these amendments to the specification are deemed to render the Examiner's objections to Figs. 1-3 moot.

The Examiner has further properly objected to the specification as failing to provide the required information with regard to the listed cross-referenced, co-pending, commonly assigned application. The specification has been amended to provide the required information. Because the Examiner's Official Action suggests that this amendment will completely dispose of the rejection of claims 3-5, 8-10, 13-14, and 18-20 under 35 U.S.C. 112, first paragraph, Applicant deems it unnecessary and unhelpful to submit further evidence of enablement at this time.

The Examiner has rejected claims 1, 2, 6, 7, 11, and 16 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,925,114, issued to Hoang (hereinafter referred to as "Hoang"). This ground of rejection is respectfully traversed for the following reasons.

"It is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention, and

that such a determination is one of fact." *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81, 90 (Fed. Cir. 1986). Hoang does not contain "every element of the claimed invention".

Specifically, with regard to claims 1 and 11 the Examiner states:

> ....a plurality of emulation objects (Figure 3 Items 332, 334 and 316, wherein each of said emulation objects emulates operation of a different one of a plurality of target processors (Figure 3, Item 332, 334, Col. 3 Lines 50-59, Col. 4 Lines 45-59, Col 6 Lines 43-56) has a software architecture different from said first software architecture (Col. 6 Lines 1-22).

This statement contains numerous findings of fact which are clearly erroneous.

First, Fig. 3, Item 316, is not an "emulation object". Fig. 3 identifies it as "Serial VxD". Column 4, lines 6-7, further define Item 316 stating:

> ....serial VxD 316, part of the OS infrastructure 310,....

Serial VxD 316 is that module within the Operating System which provides the software interface to the hardware UART 317. Item 316 is specifically not an "emulation object" as is limiting of the claims.

Second, Fig. 3, items 332 and 334 are not emulation objects "wherein each of said emulation objects emulates operation of a different one of a plurality of target processors". Item 332 is

identified in Fig. 3 as "16550 UART VxD". Column 3, lines states:

> The UART VxD 332 is a software emulation of a conventional UART...

Those of skill in the art will recognize that UART means Universal Asynchronous Receiver/Transmitter. In essence, a UART is a serial-to-parallel and parallel-to-serial converter. It is a specific piece of hardware which is not a "target processor" as required by the claimed invention.

Similarly, Item 334 of Fig. 3 is identified as "Soft Modem VxD". In short, it is a "software modem", which can be thought of as an emulation of a hardware modem. It is not emulation of a "target processor" as is required by Applicant's claim language.

Thus, the Examiner has shown that Hoang discusses emulation of hardware elements which are not "target processors", wherein Item 332 emulates a UART and Item 334 emulates a hardware modem. Item 316 is not an emulation at all. Therefore, Hoang does not have the "plurality of emulation objects" which emulate different ones of a "plurality of target processors".

Third, because none of Items 316, 332, or 334 emulates a "target processor", none of these Items can emulate operation of a target processor having "a software architecture different from said first software architecture. Instead, the Examiner cites

column 6, lines 1-20, which describe a different and mutually exclusive software architecture for the entire system of Hoang.

Therefore, the rejection of claims 1 and 11 is respectfully traversed as based upon clearly erroneous findings of fact and without these clearly erroneous findings, Hoang does not "meet every element of the claimed invention" as is required by controlling law.

In rejecting claims 6 and 16, the Examiner surprisingly states:

> As regards independent Claims 6 and 16 the Hoang reference discloses an apparatus (Figure 1).

Because this apparently constitutes the entire basis for the rejection, it is not readily apparent whether the Examiner assumes that this statement is procedurally sufficient or whether the Examiner is somehow relying upon clearly erroneous findings of fact made with regard to the rejection of claim 1 and 11. In either case, the rejection of claims 6 and 16 is respectfully traversed as at least being procedurally inadequate.

Failing to acknowledge that claims 2 and 7 are different, have different elements, and have differing scopes, the Examiner seeks to reject them both by stating:

> As regards Claims 2 and 7 the Hoang reference discloses and (sic) emulation object and a computer program that are compatible with the first software architecture (Figure 3, Col. 3 Lines 60-67, Co. 4 Lines 1-7).

Nevertheless, the cited text does not meet the claimed elements of either claim as required by controlling law.

Claims 3-5, 8-10, 12-15, and 17-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Hoang in view of U.S. Patent No. 5,379,432, issued to Orton et al (hereinafter referred to as "Orton") and further in view of U.S. Patent No. 5,574,927, issued to Scantlin (hereinafter referred to as "Scantlin"). This rejection is respectfully traversed for failure of the Examiner to present a *prima facie* case of obviousness as required by MPEP 2143.

In accordance with MPEP 2143, the Examiner is required to show the that alleged combination of Hoang, Orton, and Scantlin are: 1)motivated; 2)reasonably likely to succeed; and 3)contain all of the claimed elements. The Examiner has failed to make any of these three showings with regard to the alleged combination.

With regard to the need to show all of the claimed elements, as explained above, Hoang, of the alleged combination, does not have the elements of the claims from which claims 3-5, 8-10, 12-15 and 17-20 depend. Furthermore, the alleged combination does not show the elements unique to these claims, which are admitted by the Examiner to not be found in Hoang.

The Examiner states:

> The Orton et al. reference discloses procedure calls (Figure 2, Item 208).

This statement is clearly erroneous as a matter of fact and is irrelevant as a matter of law. Though Item 208 states, "Procedural Function Call", it does not disclose "procedure calls" as stated by the Examiner. Furthermore, because the claims are limited to an "array of procedures", the statement, even if true, would be irrelevant. Orton certainly has no "array of procedures".

Similarly, the Examiner states:

> The Scantlin reference discloses a list of instructions compatible with a second software architecture (Figure 3, Item 28).

Again, this is clearly erroneous as a matter of fact. Item 28 is a piece of hardware labeled "Target Instruction Decode and Dispatch". It contains hardware registers R10, R11, and R12. It is clearly not a "list of instructions" as is limiting of the claims.

Having thus failed to make the required showing that the alleged combination have all of the claimed elements, the Examiner completely ignores his obligation to present evidence of reasonable likelihood of success. As a matter of fact, one probably could not perform the Hoang software emulation of a modem using the Object-oriented interface of Orton, and one could certainly not do so employing the hardware emulation technique of Scantlin. There is no reasonable likelihood of success.

The remaining requirement is that the Examiner present evidence to show motivation. He has not done so. Instead, he has simply concluded that motivation exists. In fact it would not be obvious to utilize the Object-oriented approach of Orton, because it would be too inefficient for emulating the modem of Hoang. Furthermore, the software emulation of Hoang and hardware emulation of Scantlin are mutually exclusive approaches.

The rejection of claims 3, 9, 15, 17, and 18 is respectfully traversed for failure of the Examiner to make any of the three showings required by MPEP 2143 to present a *prima facie* case of obviousness.

In rejecting claims 4, 8, 13, 14, 19, and 20 the Examiner again fails to make the three showings required by MPEP 2143. In addition to his lack of showing of reasonable likelihood of success and unsupported mere conclusion of motivation, his findings of fact are legally irrelevant because he fails to address the claimed limitations. For Applicant's definition of the claimed "specialized instructions for communications processing", the Examiner's attention is directed to the specification at page 1, line 17, through page 2, line 3. The rejection of claims 4, 8, 13, 14, 19, and 20 is respectfully traversed for failure of the Examiner to make a *prima facie* case of obviousness as described in MPEP 2143.

In his rejection of claim 5 the Examiner disingenuously states:

> As regards Claim 5 the Hoang reference does not expressly disclose an array of procedures corresponds (sic) to a list of instructions selected by using an operation code and a corresponding four-bit field.

As the Examiner is well aware, the alleged combination of prior art references does not disclose "an array of procedures". Furthermore, the Examiner does not even allege that it does. Therefore, it would seem to be dishonest for the Examiner to allege that the combination somehow contains the claim limitation. Instead he makes a finding of fact which is legally irrelevant, because it is not directed to the claimed invention. The rejection of claim 5 is respectfully traversed.

The Examiner similarly mis-examines claim 10. The claim is actually limited by: "each of said procedures of said array of procedures is directly linked to a different one of said list of instructions". Instead of addressing the claim limitation, the Examiner states:

> The Scantlin reference discloses an array of instruction directly linked to a different set of instructions.

Though this finding of fact is clearly erroneous, the finding is legally irrelevant because it does not address the claimed limitations. The rejection of claim 10 is respectfully traversed.

Claim 12 depends from claim 11 and is further limited by "repeating step b for each of said plurality of target processors". Having found that Hoang anticipates claim 11, the Examiner surprisingly contradicts his own anticipation rejection of claim 11 by stating:

> As regards Claim 12 the Hoang reference does not expressly disclose multiple target processors.

Having already found that Hoang did "expressly disclose multiple target processors", the Examiner intentionally and knowingly disputes his own anticipation rejection of claim 11.

In an apparent attempt at compounding the error, the Examiner states:

> The Scantlin reference discloses a plurality of target processors.

And almost immediately contradicting that finding by stating:

> ....the Scantlin reference discloses a method of emulating the instruction execution of <u>one</u> type of processor on another. (Emphasis added)

Actually, the Examiner is correct the second time. Scantlin shows the emulation of a single target processor (see the title, for example). The rejection of claim 12 is respectfully traversed.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By his attorney,

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